CLEAN COPY OF THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-12. (canceled)

13. (previously presented) A memory cell comprising:

a plurality of access transistors having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first storage transistor is coupled between the storage node and a power supply node and its gate coupled to the complement storage node, and a second storage transistor coupled between the complement storage node and the power supply node and its gate coupled to the storage node; and

a control circuit coupled to monitor voltage on the storage node, compare the monitored voltage on the storage node with a reference voltage and in response, to generate a tracking voltage coupled to the wordline to adjust leakage current through the access transistors to exceed leakage through the plurality of storage transistors.

14. (previously presented) The memory cell of claim 13 wherein the reference voltage is programmable.

15. (previously presented) The memory cell of claim 13 wherein the tracking voltage is to be maintained substantially constant.

16. (previously presented) The memory cell of claim 15 wherein the tracking voltage is buffered to substantially reduce disturbances caused by switching of the input signal on the wordline.

17. (previously presented) The memory cell of claim 15 further comprising a plurality of partial memory cells, each partial memory cell having at least one access transistor and at least one storage transistor to operate as a dummy cell, and the control circuit to monitor a dummy storage node of the dummy cell to compare to the reference voltage to generate the tracking voltage on the wordline.

18-19. (canceled)

20. (previously presented) A method to maintain a leakage current ratio between access and storage devices in a memory cell comprising:

establishing a reference voltage that corresponds to an output voltage of the memory cell;

generating a tracking voltage in response to comparing the reference voltage with an output voltage of a dummy cell; and

coupling the tracking voltage to a location in the memory cell to control leakage current in the access device to be greater than leakage current in the storage device.

21. (previously presented) The method of claim 20 further including using the tracking voltage to vary well to substrate bias voltage of the storage device to control the leakage current through the storage device.

22. (previously presented) The method of claim 20 further including using the tracking voltage to vary bias on a node coupled to a supply rail to control the leakage current through the storage device.

23. (previously presented) The method of claim 20 further including using the tracking voltage to adjust voltage on a wordline of the memory cell to vary gate bias of the access device to adjust the leakage current through the access device.

24. (previously presented) The method of claim 23 further including buffering the tracking voltage.

25. (previously presented) A memory cell comprising:

a plurality of access transistors having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first storage transistor is coupled between the storage node and a power supply node and its gate coupled to the

complement storage node, and a second storage transistor coupled between the complement storage node and the power supply node and its gate coupled to the storage node; and

a control circuit to generate a tracking voltage that corresponds to a voltage on the storage node and to couple the tracking voltage to a substrate well of the first and second storage transistors to provide a well-substrate bias for the storage transistors to ensure that leakage current through the two storage transistors does not exceed leakage current through the two access transistors.

26. (previously presented) The memory cell of claim 25 further comprising a plurality of partial dummy memory cells that are placed in a state which mimics a stored state of the storage transistors and in which stored state voltage from the dummy memory cells are to be used to generate the tracking voltage.

27. (previously presented) The memory cell of Claim 26 wherein the tracking voltage is a function of the stored state voltage from the dummy cells and a reference voltage.

28. (previously presented) A memory cell comprising:

a plurality of access transistors having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first storage transistor is coupled between the storage node and a power supply node and its gate coupled to the complement storage node, and a second storage transistor coupled between the complement storage node and the power supply node and its gate coupled to the storage node; and

a control circuit to generate a tracking voltage that corresponds to a voltage on the storage node and to couple the tracking voltage to a power supply node of the first and second storage transistors to provide a bias for the storage transistors to ensure that leakage current through the two storage transistors does not exceed leakage current through the two access transistors.

29. (previously presented) The memory cell of claim 28 further comprising a plurality of partial dummy memory cells that are placed in a state which mimics a stored state of the storage transistors and in which stored state voltage from the dummy memory cells are to be used to generate the tracking voltage.

30. (previously presented) The memory cell of Claim 29 wherein the tracking voltage is a function of the stored state voltage from the dummy cells and a reference voltage.